Notice of Allowability	Application No.	Applicant(s)	
	10/082,077	NI, SHIH-HSIUNG	
	Examiner	Art Unit	
	Chirag G. Shah	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/26/07*.

2. ☒ The allowed claim(s) is/are *1-56*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

CHIRAG G. SHAH
PRIMARY PATENT EXAMINER

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claim 49, line 7, "multipleindependent" has been replaced with "multiple independent".

Claim 50, line 3, "thedata" has been replaced with "the data".

Reasons For Allowance

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, Prior art fails to disclose a look-ahead logic module configured to select an address of a first memory bank of an external memory device, wherein the look-ahead logic module is contained within an internal memory control device located within the communication device; a pointer assignment module, connected to the look-ahead module, is configured to include an independent link list assigned exclusively to the first memory bank and to assign a pointer to the data packet based upon the first memory bank as determined by the look-ahead logic in combination with other limitations set forth in the respective claim.

Regarding claim 8, Prior art fails to disclose a look-ahead logic module configured to override and assign a swapping address mapping scheme to select an

address of a first memory bank of a memory device so that the data packet will not be assigned to a memory bank accessed in a previous request operation wherein the look-ahead logic module is contained within an internal memory control device located within the communication device; a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 15, Prior art fails to disclose a look-ahead logic module configured to select an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank wherein the look-ahead logic module is contained within an internal memory control device located within the communication device; a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 19, Prior art fails to disclose a link list configured to include multiple independent link lists, wherein each link list is assigned exclusively to a predetermined memory bank located within the communication device; a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer from one of the independent link lists to the data packet based upon the first memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 23, Prior art fails to disclose selecting an address of the memory bank of the external memory bank so that the data packet will not be assigned to a memory bank accessed in a previous request operation and assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic in combination with other limitations set forth in the respective claim.

Regarding claim 30, Prior art fails to disclose overriding a swapping address mapping scheme to select and assign an address of the memory bank of the memory device so that the data packet will not be assigned to a memory bank accessed in a previous operation and assigning a pointer to the data packet based upon the address of the memory bank determined in combination with other limitations set forth in the respective claim.

Regarding claim 31, Prior art fails to disclose selecting an address of the memory bank of the memory device so that no two successive request operations access the same memory bank and assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 35, Prior art fails to disclose providing a link list configured to include multiple independent link lists, wherein each link list is assigned exclusively to a predetermined memory bank and assigning a pointer from one of the independent link lists to the data packet based upon the memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 37, Prior art fails to disclose selecting an address of the memory bank of the external memory bank so that the data packet will not be assigned to a

memory bank accessed in a previous request operation and assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic in combination with other limitations set forth in the respective claim.

Regarding claim 44, Prior art fails to disclose overriding means for overriding a swapping address mapping scheme to select and assign an address of the memory bank of a first memory device so that the data packet will not be assigned to the memory bank accessed in a previous request operation and assigning means for assigning a pointer to the data packet based upon the address of the memory bank determined in combination with other limitations set forth in the respective claim.

Regarding claims 45 and 49, Prior art fails to disclose selecting means for selecting an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank and assigning means for assigning a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claim 51, Prior art fails to disclose a look-ahead logic module configured to select an address of a first memory bank of a memory device by overriding an address mapping scheme that permits successive data packets to be assigned to the same memory bank, wherein the look-ahead logic module is contained within an internal memory control device located within the communication device and a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Regarding claims 53 and 55, Prior art fails to disclose receiving the data packet at an input port of a communication device; selecting an address of the memory bank of the memory device by overriding an address mapping scheme that permits successive data packets to be assigned to the same memory bank; assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic module in combination with other limitations set forth in the respective claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cgs
June 5, 2007

CHIRAG G. SHAH
PRIMARY PATENT EXAMINER

Chirag G. Shah
Primary Examiner, 2616